REMARKS

This application has been reviewed in light of the Office Action mailed on September 7, 2004. Claims 1-19 are pending in the application. Claims 1, 2, 5 and 8 are in independent form. By the present amendment, the Specification and Claims 1, 5 and 8 have been amended. No new matter or issues are believed to be introduced by the amendments.

(1) In the Office Action, the Examiner objected to the Specification for a number of informalities. The Specification has been amended in a manner which is believed to obviate the rejection. Accordingly, withdrawal of the rejection is respectfully requested.

(2) In the Office Action, Claims 5-9 were rejected under 35 U.S.C. §112, second paragraph. While the Examiner rejects Claims 5-9, specific rejections were only provided with regard to Claims 5 and 8. In response, Claims 5 and 8 have been amended in a manner which is believed to overcome the rejection. Accordingly, withdrawal of the rejection is respectfully requested.

(3) In the Office Action, Claim 1 was rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,754,294 issued to Adireddy et al. on June 22, 2004 ("Adireddy et al."). The rejection with respect to Claim 1 is traversed.

Applicant's invention provides a method and corresponding circuitry for mitigating performance loss (i.e., removing unwanted latency) caused by feedback loop

delay in a decision feedback equalizer. In the preferred embodiments according to the invention, a small delay compensation filter (i.e., an N-tap filter) is used in parallel with a feedback equalizer (see Figs. 4 & 5 of specification). The feedback equalizer is part of a first feedback loop and the N-tap filter is part of a second feedback loop. The length of the N-tap filter is equal to the number of the implementation delay introduced by the feedback equalizer loop (i.e., the unwanted symbol delay). The second feedback loop, including the N-tap filter, is free of any implementation delay associated with the first feedback loop. For example, in the case where the feedback equalizer loop requires 2 symbol times (i.e., the number of the implementation delay introduced by the first feedback equalizer loop) to compute an output result, the N-tap filter (part of the second feedback loop) is configured as a 2-tap filter, N=2. Accordingly, a first feedback signal, output from the first feedback loop, includes implementation delay while a second feedback signal, output from the second feedback loop, is free of the implementation delay.

The operation of the improved feedback equalizer of the invention can be best understood by conceptualizing it as a single FIR filter with 100 taps to which coefficients C1 to C100, respectively, are implemented in two stages. A first stage is implemented in a feedback equalizer (first loop), as described above, implementing coefficients C3 to C100 and a second stage small delay compensation filter (i.e., N-tap filter) (second loop) implemented in fast logic to minimize implementation delays. The coefficients implemented in the N-tap filter can be selected to optimize the processing of postcursor echoes that are very close to the main path.

In the Office Action, the Examiner alleges that Adireddy et al. discloses in (Fig. 4), a first feedback equalizer signal (415, 420) and a second feedback equalizer signal (430, 435) for controlling a decision feedback equalizer, wherein the first feedback equalizer signal is delayed by an implementation delay and wherein the second feedback equalizer signal is free of the implementation delay.

Adireddy et al. is directed to an apparatus for reducing a precursor ISI signal in a receiver that receives an incoming stream of symbols distorted by intersymbol interference (ISI) (see Adireddy et al. at Col. 2, lns. 55-60). Fig. 4 illlustrates an exemplary precursor cancellation feedback filter (PC-DFE). The (PC-DFE) includes, inter alia, symbol estimator 415, feedback filter 420, a known symbol generator 430 and feedback filter 435. The Examiner alleges that the symbol estimator (415) and feedback filter (420) discloses a feedback equalizer signal delayed by an implementation delay. The Examiner further alleges that the known symbol generator (430) and feedback filter (435) discloses a feedback equalizer free of any implementation delay.

Independent Claim 1 has been amended herein to better define Applicant's invention over Adireddy et al. Claim 1 now recites limitations and/or features which are not disclosed by Adireddy et al.

Claim 1 as amended herein recites:

1. First and second feedback equalizer signals for controlling a decision feedback equalizer, wherein the first feedback equalizer signal is **output from a first feedback loop and is** delayed by an implementation delay and wherein the second feedback equalizer signal is **output from a second feedback loop and is** free of the implementation delay, **wherein said first and second feedback loops process decisions**

from a decision device common to both of said first and second loops.

Adireddy does not disclose or suggest: *the second feedback equalizer signal is output from a second feedback loop and is free of the implementation delay, wherein said first and second feedback loops process decisions from an output of a single decision device sourcing both first and second loops.*

Adireddy, shows the alleged "feedback equalizer" (430, 435) receiving a timing signal and outputs a sequence of known symbols, S_k through feedback filter 435 at the proper location in the sequence of known and unknown symbols that are being processed by symbol estimator 415. The alleged "feedback equalizer" (430, 435) is not part of, nor does it constitute either a first or second feedback loop, as recited in Claim 1, as amended.

As a further distinction, Adireddy et al. only discloses a single feedback loop. Namely, the loop constituting output S_{k-d} feeding feedback filter 420 whose output sources adder 425. Accordingly, Adireddy et al. does not disclose *.first and second feedback loops process decisions from an output of a single decision device sourcing both first and second loops*, as recited in Claim 1.

As yet another distinction, it is submitted that all of the feedback filters shown in Fig. 4 of Adireddy et al. (i.e., 430, 435) inherently add implementation delay. That is, there is no teaching in Adireddy that any of the feedback filters (430, 435) are free of implementation delay. Applicant cannot find any teaching or disclosure in Adireddy et al. disclosing such a feature.

It is respectfully submitted that at least the limitations and/or features of Claim 1 which are underlined and italicized above is not anticipated by the disclosure of Adireddy et al.

Accordingly, withdrawal of the rejection under 35 U.S.C. §102(e) with respect to Claim 1 and allowance thereof is respectfully requested.

Claims 2-4 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,754,294 issued to Adireddy et al. on June 22, 2004 ("Adireddy et al.") in view of U.S. Patent No. 5,020,078 issued to Crespo on May 28, 1991 ("Crespo").

With regard to Claim 2, the Examiner alleges that Adireddy et al. discloses a decision feedback equalizer (DFE) comprising a forward equalizer; first and second adders; a decision device; a feedback equalizer. The first and second adders, the decision device and the feedback equalizer constituting a first feedback loop. The second feedback loop is free of an implementation delay associated with the first feedback loop.

In rejecting Claim 2, the Examiner correctly notes that Adireddy et al. does not disclose an N-tap filter (61); the second adder (57); the decision device (44); and the N-tap filter (61) constitute a second feedback loop, and N is a positive integer. Crespo is cited in attempt to remedy this deficiency. It is respectfully submitted that Crespo does not show an N-tap filter (61). Rather, Crespo merely shows the delay elements of a filter, i.e., delay elements 45-48.

Further, the recited elements do not function as a feedback loop in Crespo as alleged in the office action. As shown in Fig. 3 of Crespo, the output of adder 57 is applied to subtractor 58 which outputs an error signal e(k) used to adaptively adjust the multiplier coefficients to minimize the mean-square error $E[e(k)^2]$ between the delayed

impulse response s(k) and the output z(k) of the transversal filter 61-62. A feedback loop, by definition, feeds back some of the output signal back to the input of a circuit. The adjustment of multiplier coefficients does not constitute a feeding back of some of the output signal back to the input of the circuit. If, for example, output z(k) of adder 57 were to be supplied as one input to subtractor 43, this may constitute a feedback loop.

Further, the Examiner alleges that Crespo teaches that the second loop is free of an implementation delay at Col. 9, lines 7-21, wherein it is stated:

> The difference is applied to threshold detector 79 to generate an indication that the c_1 is greater or less than .alpha.c_0. Counter control circuit 80 uses the output of threshold detector 79 to control counter divider 81. Counter 81 is driven by master clock 82, to count down the pulses from clock 82 and apply every nth pulse to operate sampling gate 70. Clock 82 and counter 81 are selected to produce sampling pulses at the nominal pulse rate of the transmitted pulse train. Counter control 80, however, is able to alter the count in counter 81 by one count at a time, either up or down. By so adjusting the count in counter 81, the control circuit is able to adjust the phase of the sampling pulse. The fineness of this adjustment is determined by the maximum count of counter 81.

Applicant fails to see how the disclosure above has any relevance whatsoever to implementation delay.

For the reasons given above, the cited references, alone or in combination, do not anticipate the subject matter of Claim 2. That is, none of the cited references taken alone or in any proper combination disclose or suggest a second feedback loop, nor one that is free of implementation delay.

Accordingly, applicants respectfully request that the rejection under 35 U.S.C. §103(a) with respect to Claim 2 and allowance thereof is respectfully requested.

Additionally, Claims 3 and 4 depend from independent Claim 2 and therefore contain the limitations of Claim 2. Hence, for at least the same reasons given for Claim 2, Claims 3 and 4 are believed to be allowable over the cited references.

Further, Claim 3 is believed to contain patentable subject matter in its own right. In the Office Action, the Examiner alleges that Crespo teaches wherein the N-tap filter is implemented in fast logic. Applicant respectfully disagrees. Crespo teaches at Col. 7, lines 64-68 and Col. 8, lines 1-9 that a training sequence is available only for the initial set up of coefficient values. A training source produces a known sequence of pulse signals used to adjust the multiplier coefficient values. At the end of the sequence, the delay line is then switched from the training source to an output of detector 44. Claim 3 recites: 3. The DFE as recited in claim 2, wherein the N-tap filter is implemented in fast logic. This means that the loop closed by the N-tap filter of the invention can be completed within one symbol period, including tap adaptation. Crespo, at best is teaching tap adaptation only.

Accordingly, withdrawal of the rejection under 35 U.S.C. §103(a) with respect to Claims 3 and 4 and allowance thereof is respectfully requested.

In view of the foregoing amendments and remarks, it is respectfully submitted that all claims presently pending in the application, namely, Claims 1-9, are believed to be in condition for allowance and patentably distinguishable over the art of record.

If the Examiner should have any questions concerning this communication or feels that an interview would be helpful, the Examiner is requested to call Dicran Halajian, Esq., Intellectual Property Counsel, Philips Electronics North America, at 914-333-9607.

Respectfully submitted,

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